30.(New) The integrated circuit of claim 29, wherein said memory array is comprised of non-volatile memory cells.

31.(New) The integrated circuit of claim 29, wherein said series of values are analog values.

32.(New) The integrated circuit of claim 30, wherein said memory array comprises a FLASH EEPROM memory.

33.(New) The integrated circuit of claim 29, further comprising:

an activation circuit coupled to the input/output pin and to the sound processing circuit, wherein the sound processing circuit is activated by the activation circuit to supply said audio signal to the input/output pin in response to an input signal received from the input/output pin.

34.(New) A method for operating a sound processing unit, comprising:

connecting a terminal of a sound processing circuit to a speaker;

recording by the sound processing circuit an audio input received through the speaker;

generating an input signal to the terminal of the sound processing circuit; and

in response to the input signal, supplying from the sound processing circuit through the terminal to the speaker an output signal derived from the audio input, wherein the output signal drives the speaker to produce a sound.

35.(New) The method of claim 34, wherein said input signal is generated by creating a vibration in the speaker.

36.(New) The method of claim 34, wherein the sound processing circuit is an integrated circuit and the terminal is a bi-directional input/output pin of the integrated circuit.--

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REMARKS

These remarks are in response to the Final Office Action mailed on August 28, 2000, setting a response period expiring on November 28, 2000, and for which a two-month extension is hereby requested. In that Office Action, all of the pending claims, claims 2, 4-9,